

IN THE CLAIMS

What is claimed is:

- 1    1.    A semiconductor integrated circuit device, comprising:
- 2            a plurality of insulated gate field effect transistors (IGFETs) coupled to
- 3            a corresponding input/output (I/O) terminal through a corresponding first
- 4            resistance;
- 5            a first clamping device coupled to each I/O terminal;
- 6            a second clamping circuit corresponding to each IGFET, each second
- 7            clamping circuit including a second clamping device and the corresponding
- 8            first resistance, each second clamping device having a first terminal connected
- 9            to a gate electrode of the corresponding IGFET and a second terminal
- 10           connected to a source/drain terminal of the corresponding IGFET and a supply
- 11           potential wiring;
- 12           each first clamping device being coupled to one second clamping
- 13           device through a second resistance; and
- 14           at least two of the second clamping circuits vary from one another.

- 1    2.    The semiconductor integrated circuit device method of claim 1, wherein:
- 2            a supply potential wiring is selected from the group consisting of an
- 3            electric power supply potential wiring, a ground electric potential wiring, and a
- 4            substrate electric potential wiring.

1 3. The semiconductor integrated circuit device of claim 1, wherein:  
2 the at least two second clamping circuits vary by the second clamping  
3 device of one second clamping circuit having a different capability than the  
4 second clamping device of the other second clamping circuit.

1 4. The semiconductor integrated circuit device of claim 1, wherein:  
2 the at least two second clamping circuits vary by a first resistance ( $R_{in}$ ) of  
3 one second clamping circuit having a different value than the first resistance ( $R_{in}$ )  
4 of the other second clamping circuit, and a ratio between the second resistance  
5 and the first resistance ( $R_g/R_{in}$ ) for both clamping circuits having a  
6 predetermined maximum value.

1 5. The semiconductor integrated circuit device of claim 1, wherein:  
2 a length of a wiring that connects the second clamping devices to the  
3 gate electrode of the corresponding IGFETs is no more than 100 micrometers.

1 6. The semiconductor integrated circuit device of claim 1, wherein:  
2 a length of a wiring that connects the second clamping devices to the  
3 source/drain electrode of the corresponding IGFETs is no more than 100  
4 micrometers.

1 7. The semiconductor integrated circuit device of claim 1, wherein:  
2 the first resistance comprises essentially a wiring resistance and a





4 second clamping device of the other second clamping circuit.

1 16. A method for designing a protective circuit for a semiconductor integrated circuit  
2 device that includes insulated gate field effect transistors (IGFETs) formed thereon, the  
3 method comprising the steps of:

4 executing a simulation with a predetermined charged device model  
5 (CDM) equivalent circuit that includes a first clamping device connected to an  
6 input/output (I/O) terminal, a first IGFET having a gate connected to the I/O  
7 terminal through a first resistance ( $R_{in}$ ), a second clamping device connected  
8 between gate and source/drain terminals of the first IGFET and connected to a  
9 supply potential wiring, the first and second clamping devices being  
10 connected to one another through a second resistance ( $R_g$ ); and

11 selecting a ratio of the second resistance and the first resistance  
12 ( $R_g/R_{in}$ ) that prevents a potential between the gate and source/drain terminal  
13 of the first IGFET from exceeding a predetermined value.

1 17. The method of claim 16, wherein:

2 the predetermined value is determined from a relationship between  
3 CDM test results and ratios of the second resistance and the first resistance  
4 ( $R_g/R_{in}$ ), and simulation results showing a relationship between a potential  
5 between the gate and source/drain terminal of the first IGFET and ratios of the  
6 second resistance and the first resistance ( $R_g/R_{in}$ ).

